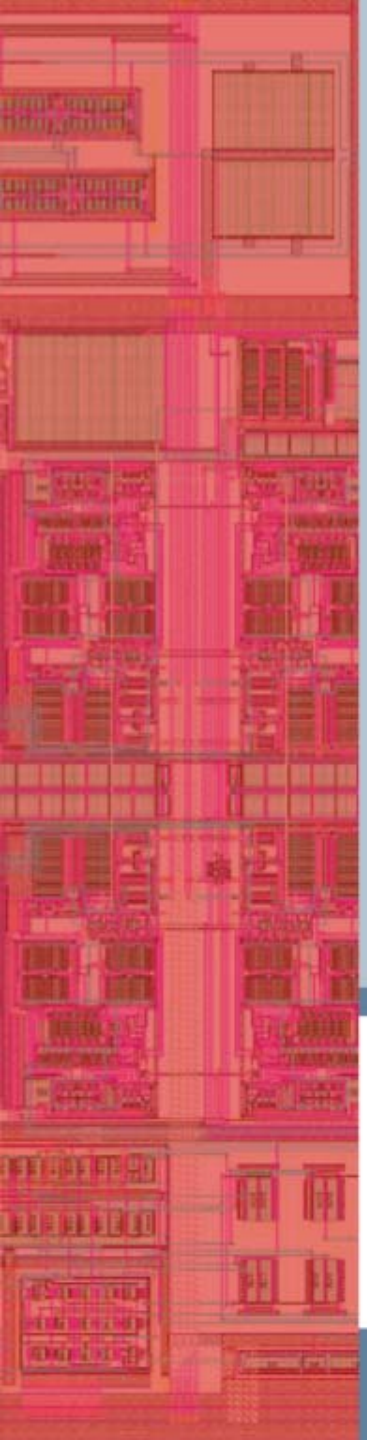


Postupak proizvodnje CMOS-a

Savetovanje / Fabrika čipova u Srbiji
Petnica, 28-29. jun 2013.

Dr Milan Savić
Dušan Grujić

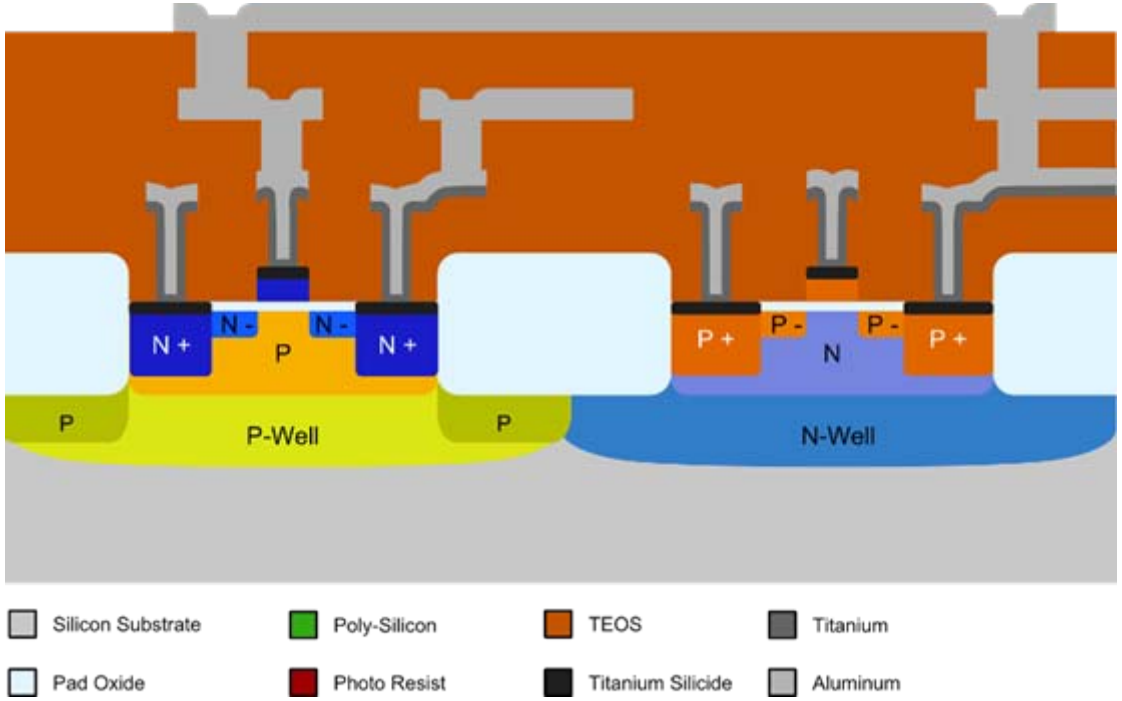
novelIC
MICROSYSTEMS

Postupak proizvodnje CMOS

- Agenda
  - Standardni koraci
  - Dodatni koraci
  - Napredne tehnike
  - Alati
  - Fotolitografija

Struktura CMOS tranzistora

standardni CMOS



Koraci u procesiranju CMOS

početni koraci

1. Početni materijal

- *Wafer* p-tipa
- Dimenzije:
  - 200 mm (8''), 725 μm
  - 300 mm (12''), 775 μm
  - 450 mm u najavi
- Epitaksijalni sloj ~ μm p-tip
- Procesiranje unutar i iznad epitaksijalnog sloja

2. Pad oksidacija i depozicija nitrida

- Oksidacija
  - Suva
  - Vlažna
    - Obično za deblje, lošiji kvalitet
  - Pećnice *(furnaces)*
    - Više wafer-a istovremeno
- *Rapid Thermal Oxidation* (RTO)
  - *Rapid Thermal Processing* (RTP) procesi
  - UV lampe, dobra kontrola
  - Kratak *ramp-up* i *-down*
  - Jedan *wafer*

- Depozicija nitrida
  - *Low-Pressure Chemical Vapor Deposition* (LPCVD)
    - Visoka temperatura
    - Degradiranje struktura usled difuzije dopanata
  - *Plasma Enhanced Chemical Vapor Deposition* (PECVD)
    - Niskotemperaturni proces
    - Koristi se kada su formirane osetljive strukture

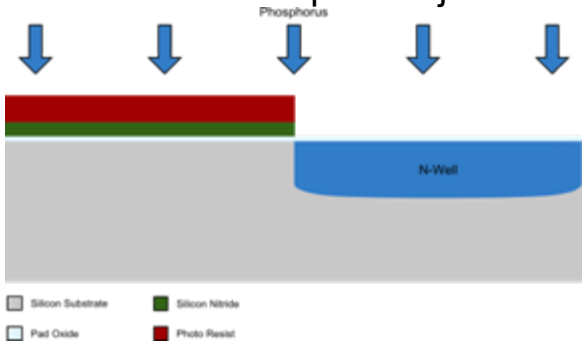
Koraci u procesiranju CMOS

formiranje *well*-a

3. N-Well foto i nagrizanje nitrida

- Fotollitografija
  - Opisana kasnije
- Nagrizanje nitrida
  - *Wet etch*
    - Vruća fosforna kiselina
    - Oksid – *etch stop layer*
    - Izotropno – loše za fine strukture
  - *Dry etch*
    - *Reactive Ion Etching* (RIE)

4. N-Well implantacija



- Difuzija
  - Difuzione pećnice
  - Dopanti
    - Nanose se (npr. PSG) ili
    - Prisutni u okruženju
  - Zagrevanje
- Jonska implantacija
  - Anizotropan proces

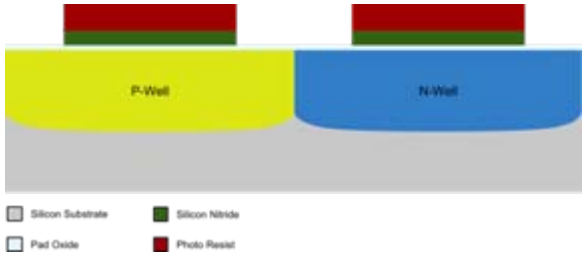
5. Uklanjanje oksida i nitrida

- Uklanjanje resista
  - Hemijski
  - *Plasma asher*
    - Posle jonske implantacije
- *Thermal Annealing*
  - Nakon implantacije
  - RTP
- Uklanjanje oksida i nitrida
  - Hemijski

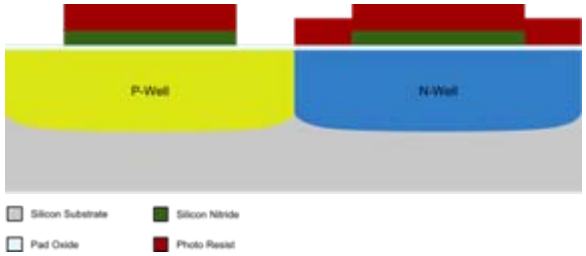
Koraci u procesiranju CMOS
izolacija

Postupak se ponavlja za formiranje p-wella, *well drive-in*, depozicija nitrida... (koraci 6 – 10)

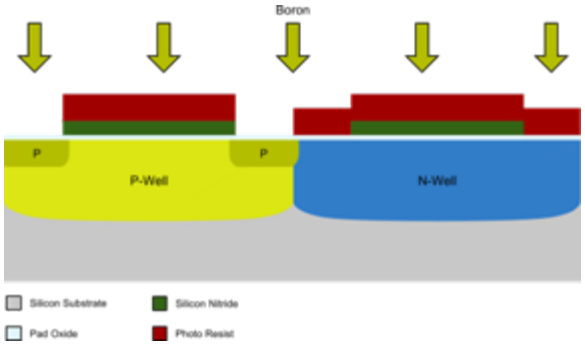
11. Foto aktivne oblasti i nagrizanje nitrida



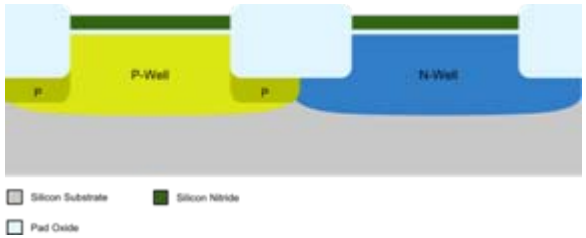
12. *p-well field* foto



13. *p-well field* implantacija



14. LOCOS okrsidacija



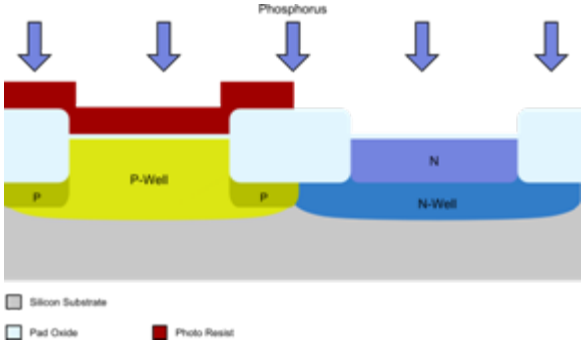
- *LOCal Oxidation of Silicon* (LOCOS)
  - *Wet* oksidacija
  - Tradicionalno

- *Shallow Trench Isolation* (STI)
  - Naprednija tehnika
  - Opisano kasnije

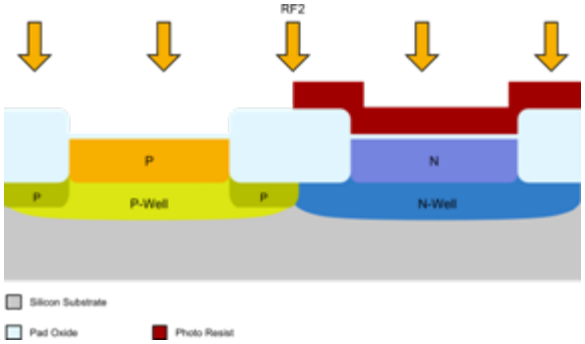
Koraci u procesiranju CMOS

podešavanje V_t

18. PMOS podešavanje V_t foto i implantacija



20. NMOS podešavanje V_t foto i implantacija

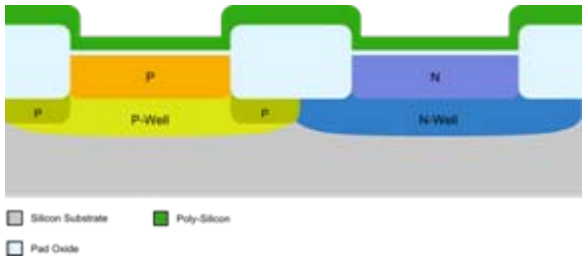


- Napon praga V_t
  - Jedan od ključnih parametara CMOS tranzistora
  - Zavisi od koncentracije dopanata u kanalu

Koraci u procesiranju CMOS

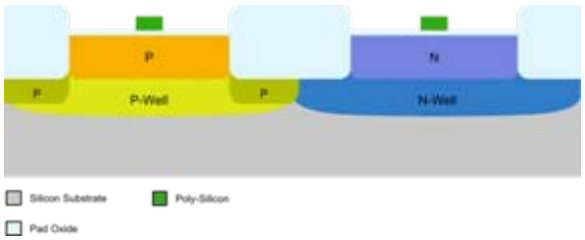
formiranje gejta I

21. Oksidacija gejta i depozicija polisilicijuma



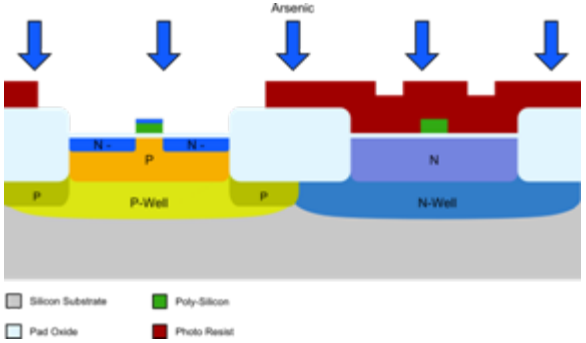
- Oksidacija gejta
  - Veoma osetljiv korak
  - Debljina oksida je ključna
  - Može biti i ispod 2 nm
  - Najnapredniji procesi: *Atomic Layer Deposition* (ALD)
- Depozija polisilicijuma
  - PECVD

22. Foto i nagrizanje gejt polija



- Nagrizanje polija
  - RIE

24. NMOS LDD foto i implantacija

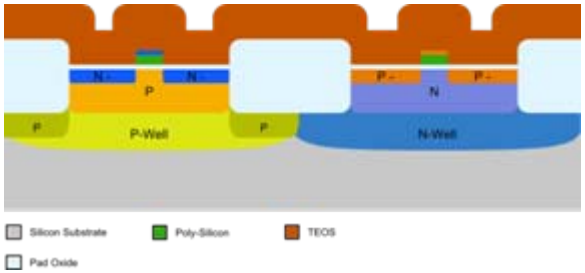


- *Lightly Doped Drain* (LDD)
- Postupak se ponavlja za PMOS

Koraci u procesiranju CMOS

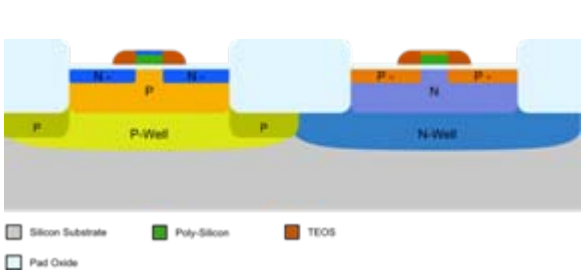
formiranje gejta II

27. Depozicija LDD *spacer*-a



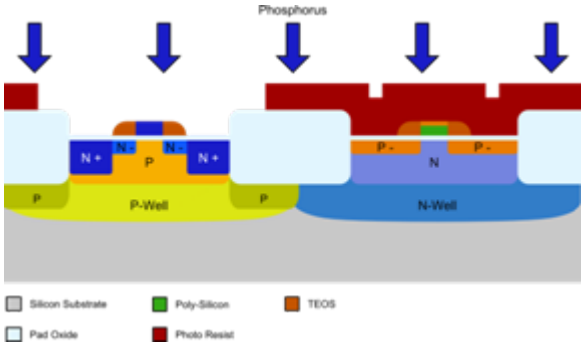
- Depozicija oksida
  - PECVD
  - Označava se sa „TEOS“
    - *Tetra Ethyl Orthosilicate* ili *Tetra Ethyl Oxysilane*
    - Prekursor za LPCVD
    - Netačno ali široko prihvaćeno

28. Formiranje LDD *spacer*-a



- Formiranje *spacer*-a
  - RIE
  - Precizno definiše D/S oblasti u odnosu na G
  - „*self-aligned*“ struktura

30. N+ S/D/G foto i implantacija

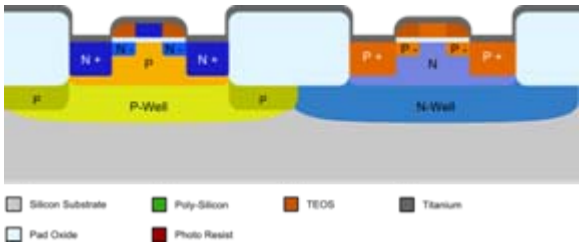


Koraci u procesiranju CMOS

formiranje *salicide*-a

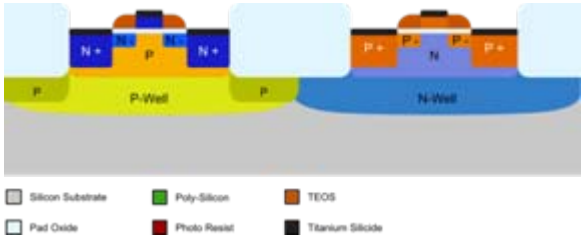
- "*Salicide*" – skraćeno od *self-aligned silicidation*.
- Silicid je jedinjenje silicijuma i metala,
- Smanjuje otpornost gejta
- Omogućuje dobar kontakt metala i silicijuma

33. Depozicija titanijuma



- Depozicija titanijuma
  - *Sputtering*
  - Pripada procesima *Physical Vapor Deposition* (PVD)

34. Formiranje titanijum silicida



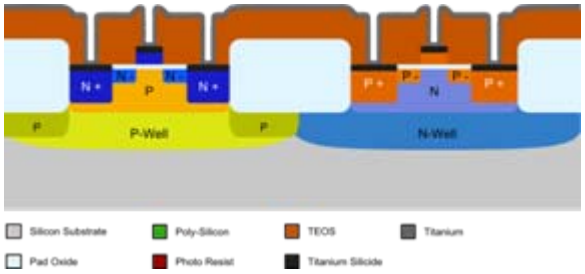
- Formiranje silicida
  - RTP

Koraci u procesiranju CMOS

BEOL – *Back-End-Of-Line*

Depozicija *TEOS*-a, foto i nagrizanje kontakata... (koraci 35, 36)

37. Depozicija titanijum *linera*-a

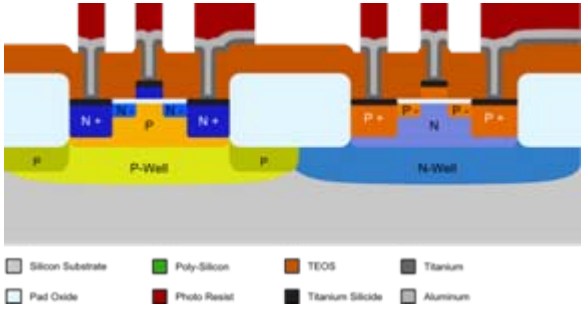


- *Liner* (Ti) / *Barrier* (TiN)
  - Ti obezbeđuje dobar kontakt
  - TiN sprečava difuziju metala u oksid
  - Debljina: mala, uniformna i ponovljiva
  - *Cluster* procesiranje

38. Depozicija aluminijuma

- Aluminijumski kontakti
  - *Sputter*
  - Tradicionalno
- *Tungsten plugs*
  - Naprednija tehnika
  - Opisano kasnije

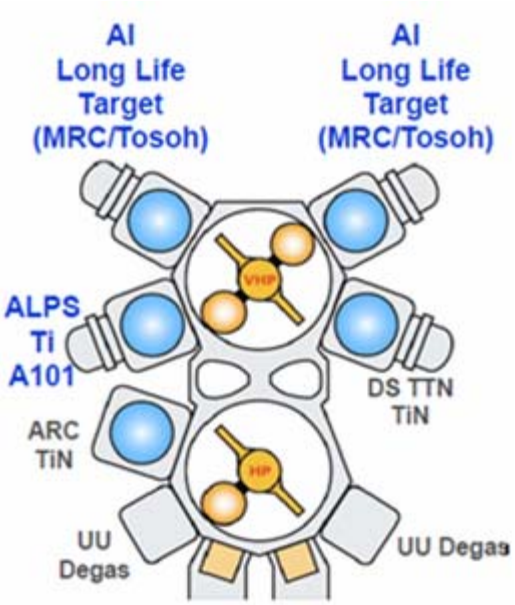
39. Metal 1 foto i nagrizanje



- Nagrizanje metala
  - *Inductively Coupled Plasma* (ICP)
  - Veća energija
  - Brže nagrizanje
  - Koristi se za metale

Koraci u procesiranju CMOS

BEOL – *Back-End-Of-Line*



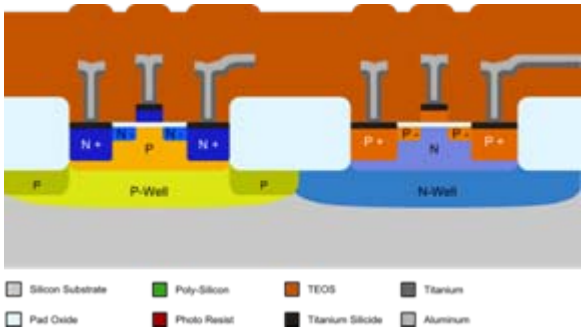
PVD Cluster – AMAT – Endura

Koraci u procesiranju CMOS

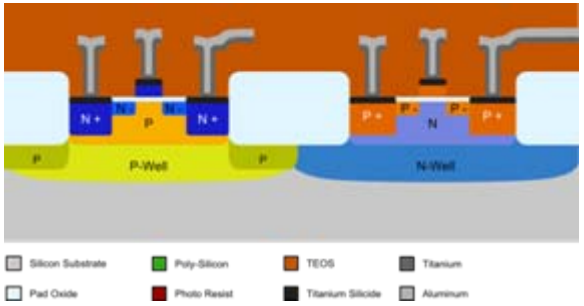
planarizacija

- Dielektrik između se označava i kao *Inter Metal Dielectric* (IMD)
- Neplanarne površine – problemi sa fokusom pri litografiji, pogoršanje kritičnih dimenzija
- Problem se pogoršava sa većim brojem metala
- IMD mora da se planarizuje pre depozicije metala za procese ≈ 0.25 µm i manje
- *Chemical Mechanical Polishing* (CMP)

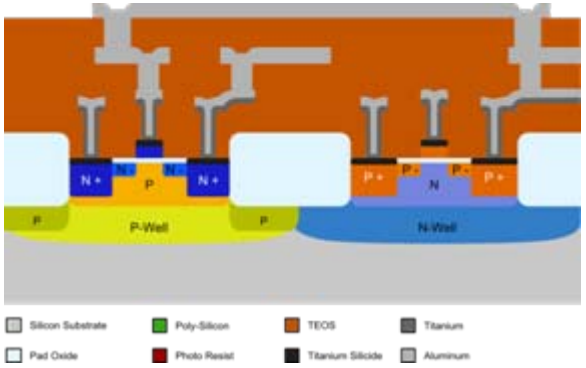
40. TEOS depozicija



41. CMP planarizacija



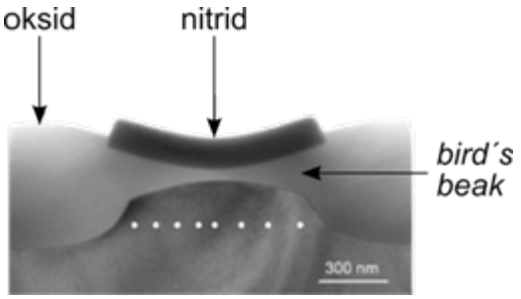
49. Kompletan CMOS



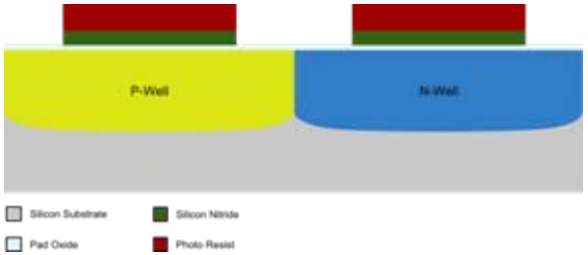
Dodatni koraci u procesiranju CMOS

STI – *Shallow Trench Isolation*

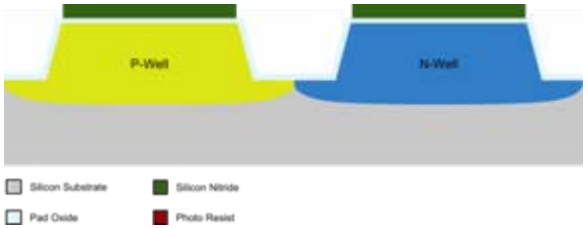
- LOCOS
  - *Bird's beak* – troši prostor
  - Nepogodan za male dimenzije
- STI – *Shallow Trench Isolation*
  - Koristi CMP



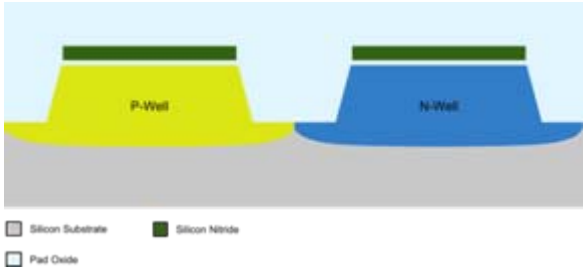
11. STI foto i nagrizanje nitrida



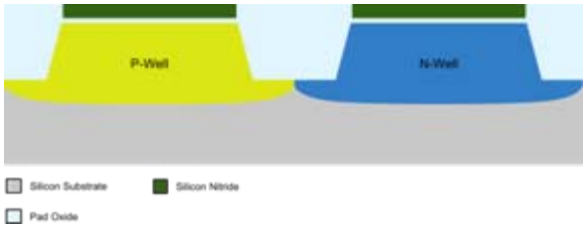
12. Nagrizanje i *liner* oksidacija



13. Depozicija oksidacija



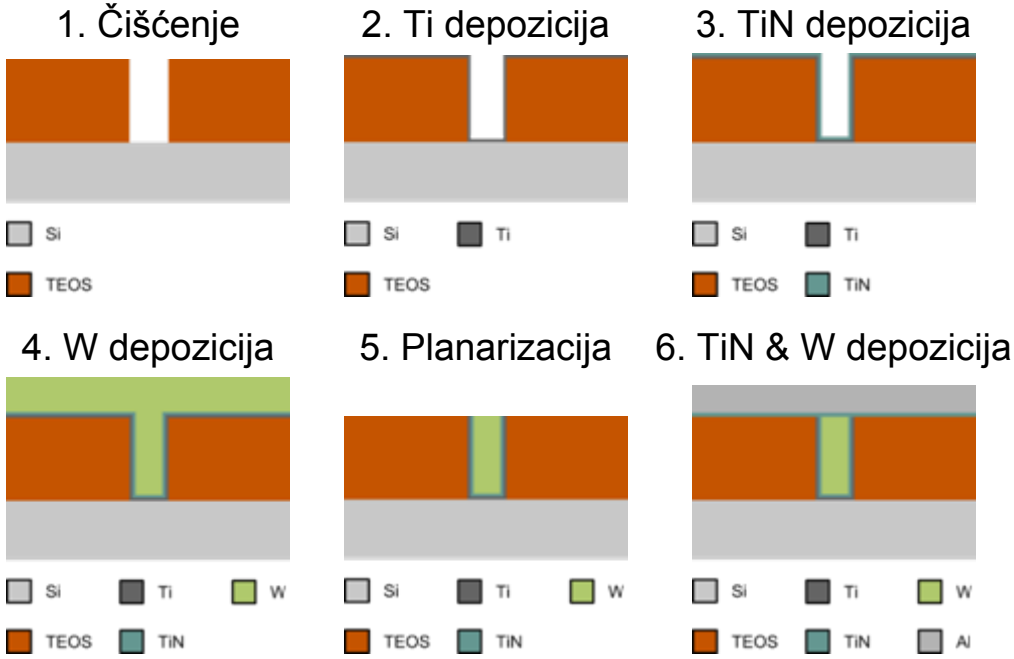
14. CMP



Dodatni koraci u procesiranju CMOS

Tungsten Plugs

- *Tungsten Plugs*
  - Zamenili su Al
  - Al *sputter* nepouzdan za male dimenzije
- Postupak
  - Ti *liner* – *sputtering*
  - Smanjuje otpornost kontakta
  - Probija oksid
  - TiN *diffusion barrier* – PVD ili CVD
  - W – LPCVD
  - Planarizacija – *etchback* ili CMP
  - WN alternativa Ti/TiN



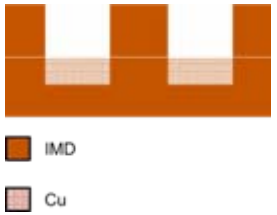
Napredni koraci u procesiranju CMOS

Damascene

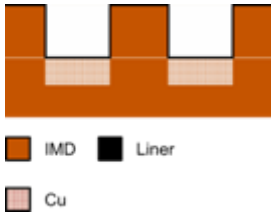
- Cilj – smanjenje RC kašnjenja interkonekcija
  - Cu / low-K umesto Al / SiO_2
  - *Low-K* – dielektrična konstanta manja nego kod SiO_2
  - Cu 40 % manja otpornost nego Al

- Metal može da se formira:
  - metal deposition → metal etching → oxide deposition → oxide polishing
  - oxide deposition → oxide etching → metal deposition → metal polishing (*damascene*)
- *Damascene*
  - Cu ne može da se nagriza
  - Cu kontaminacija Si problem → *barrier* (Ta/TaN PVD)
  - Cu depozicija – *electroplating* (ECD)
  - *Seed* – PVD – provodni film
  - Cu CMP zahtevan proces
  - Prva metalizacija – kontakt prema *Tungsten plugs*

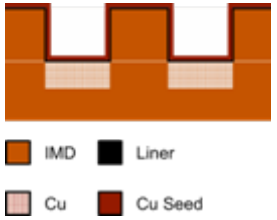
1. Nagrizanje



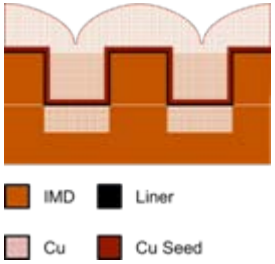
2. *Liner*



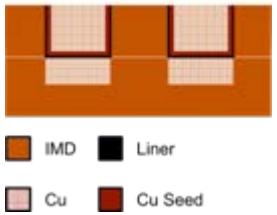
3. *Seed*



4. Cu ECD



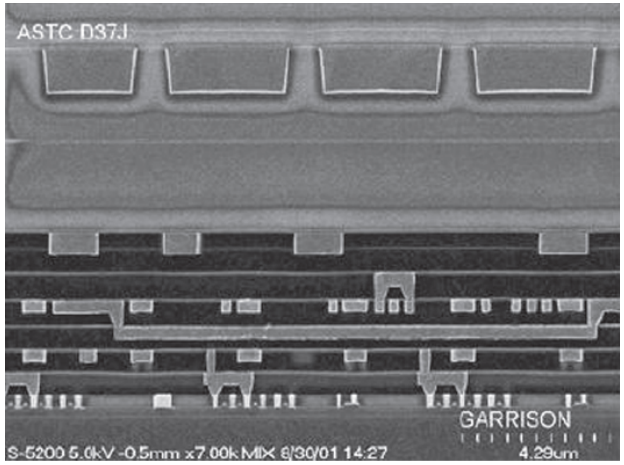
5. Cu CMP



Napredni koraci u procesiranju CMOS

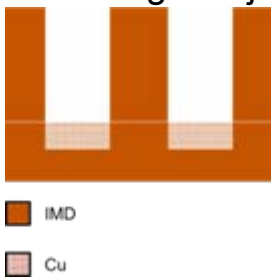
Dual Damascene

- *Dual Damascene*
  - Via i metal linije u istom koraku
  - Viši slojevi metala

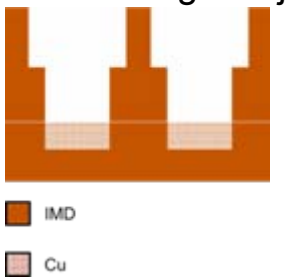


Višestruki slojevi metala (IBM)

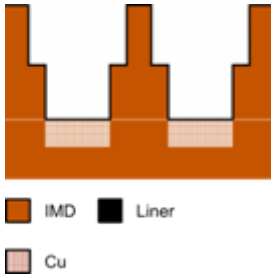
1. Via nagrizanje



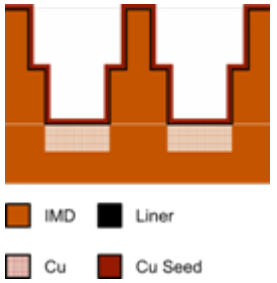
2. *Trench* nagrizanje



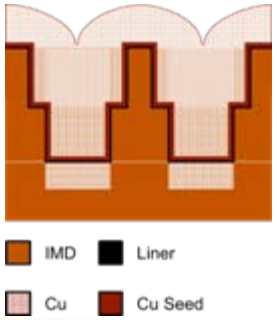
3. *Liner*



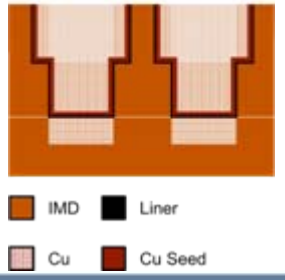
4. *Seed*



5. Cu ECD



6. Cu CMP



Napredni koraci u procesiranju CMOS

Low-K IMD; High-K gejt dielektrik

- *Low-K* IMD
  - $\varepsilon_r < \varepsilon_r (SiO_2) \approx 3,9$
  - Organski, neorganski, između
    - Slični SiO_2 :
      - *organo-silicate-glasses* (OSG)
      - *carbon-doped oxides* (CDO)
    - *Spin-on dielectric* (SOD) ili *spin-on glass* (SOG)
    - Organski dielektrici
    - *Foams*
    - *Fluorinated silicate glass* (FSG)
  - Gotovo svaki *low-k* IMD zahteva različitu depoziciju i nagrizanje
  - Smanjivanje ε_r pomoću UV (UVP)
  - Interakcija barijere, IMD i Cu je kritična u određivanju kašnjenja, pouzdanosti, elektromigracije i proboja → namenski *cluster*

- *High-K* gejt oksid
  - Deblji gejt dielektrik nego kod SiO_2 uz iste performanse
  - Manje struje curenja kroz dielektrik
  - ALD

Alati za standardni CMOS

Process Module	Equipment	Process step	Manufacturers
Lithography	Stepper		ASML (former SVG), Canon, Nikon
	Coater/Developer Track	PR spinning	Suss MicroTec
	Plasma Asher	PR removal	Axcelis Technologies (former Matrix Integrated Systems and Fusion Semiconductor), PVA TePla
	Photostabilizer	Hard bake	
Etch	Plasma Etcher	Nitride Etch	Lam Research, Applied Materials, SPTS (SPP Process Technology Systems, former STS), SPP, Primaxx, Sentech Instruments GmbH, Plasma-Therm (part of Oerlikon), Advanced Vacuum
	Plasma Etcher	Oxide/Spacer Etch	
	Plasma Etcher	Aluminum Etch	
	Plasma Etcher	Poly-Si Etch	
High Temperature Treatment	Diffusion Furnace	Gate Oxidation	Tystar
	Diffusion Furnace	Wet/dry Oxidation	AG Associates, Mattson (former Steag), Allwin21 Corp.
	Diffusion Furnace	Sintering	
	RTP	Annealing	
	RTP	Silicidation	
CVD	PECVD	TEOS Deposition	Novellus, Applied Materials, Oxford Instruments, Plasma-Therm (part of Oerlikon), Advanced Vacuum
	LPCVD	Nitride Deposition	
	LPCVD	Poly-Si Deposition	
	CVD	Tungsten Deposition	
	MOCVD	Titanium Nitride Deposition	
Thin Film Systems	Sputter System	TI Deposition	Varian/Novellus, Denton Vacuum, Oxford Instruments, Oerlikon (former Unaxis)
	Sputter System	Al Deposition	

Alati za standardni CMOS

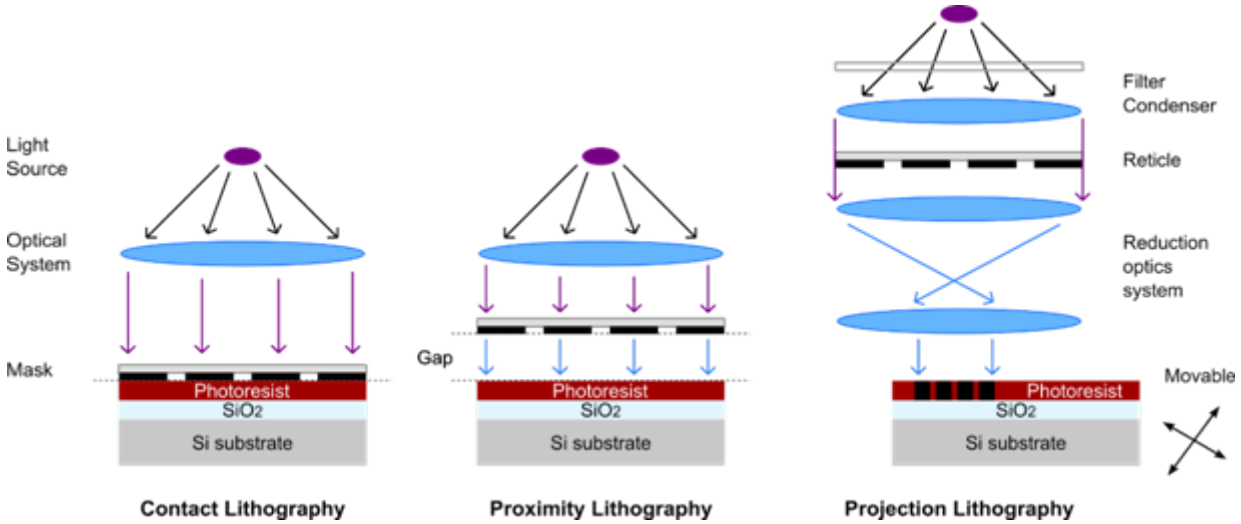
Process Module	Equipment	Process step	Manufacturers
Wet Etch and Cleaning	Sink 1	Pre-furnace piranha clean HF dip (10:1, 25:1) Rinse, spin dry	Singulus Stangl Solar GmbH PCT Systems
	Sink 2	Hot phosphoric etch Ti wet etch	
	Sink 3	Post-lithography piranha clean Buffered HF etch (5:1) Rinse, spin dry	
	Sink 4	Post-CMP clean	
Implantation	Ion Implanter	Ion Implantation	Sumitomo Eaton Nova, Varian Semiconductor Equipment Associates (VSEA), Axcelis Technologies
Metrology and Testing	Surface Profiler	Surface Profiling	KLA-Tencor
	Ellipsometer / Reflectometer	Thin Film Thickness	Nanometrics, Sentech
	SEM	Measure Channel Length	Carl Zeiss KLA-Tencor
	4-Point Measurement System	Sheet Resistance	Karl Süss, Cascade Microtech, Electroglass, Accretech
	Probe Station	Electrical Parameters	Semilab
	SCA	Gate Oxide Quality	
	Ellipsometer	Gate Oxide Thickness	
Planarization	CMP	IMD Planarization	Strasbaugh, G&P Technology
	Etchback	Tungsten Planarization	

Dodatni alati za CMOS ispod 100 nm

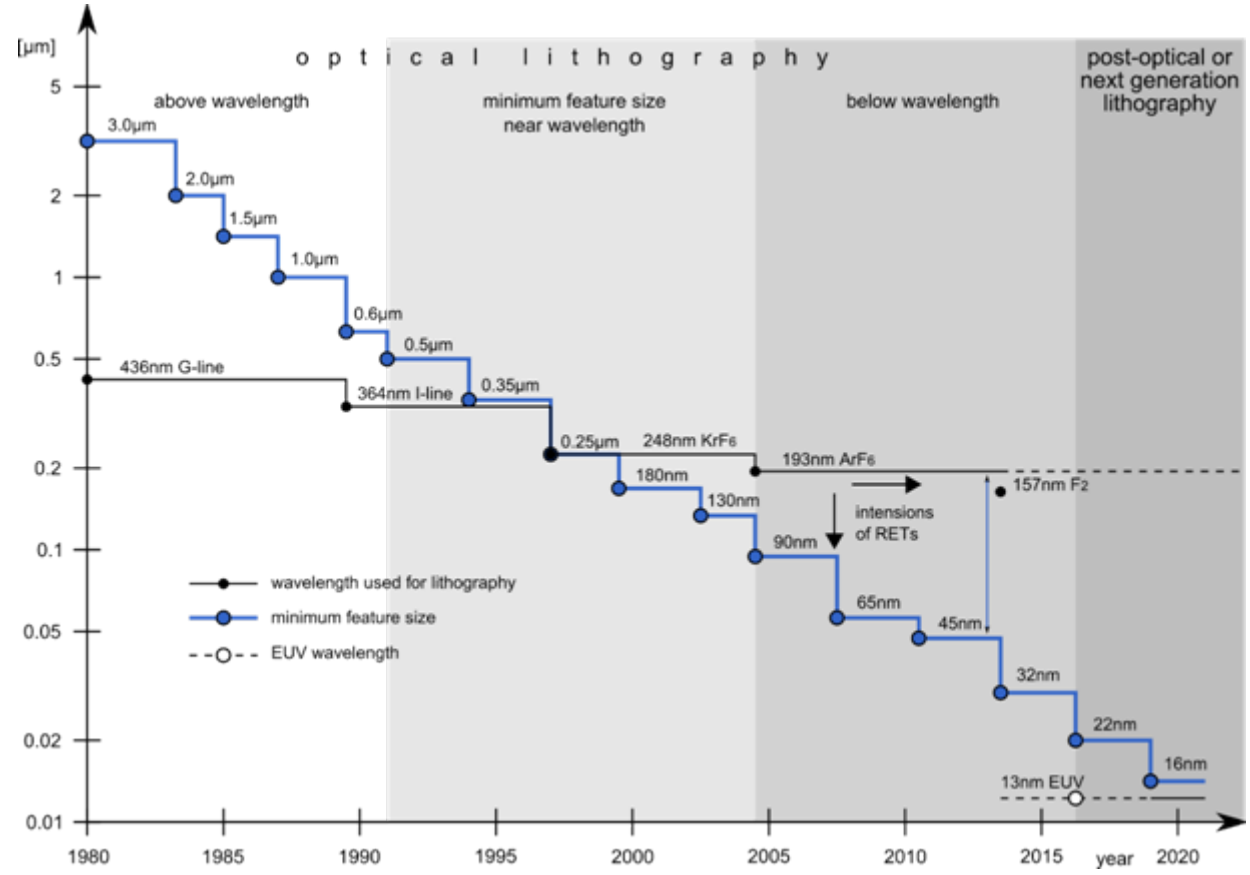
Process Module	Equipment	Process step	Manufacturers
Deposition	ECD	Copper electroplating	Novellus, Applied Materials, Semitool (now part of AMAT)
	Sputter	Cu Liner/Seed	
	PECVD	SiC Barrier	
Planarization	CMP	Copper CMP	
	CMP	Tungsten	
Cleaning		Post Cu-CMP clean	

Fotolitografija

- Fotolitografija
  - *Priming*
  - *Resist application*
  - *Soft bake*
  - *Exposure*
  - *Post exposure bake*
  - *Development*
  - *Hard bake*
  - *Stripping*



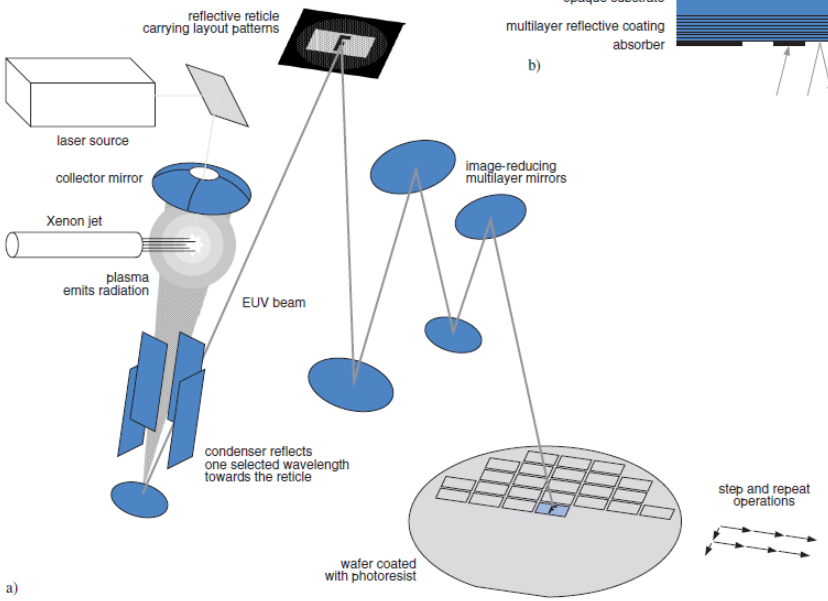
Evolucija litografije



- *Resolution enhancement techniques* (RET)
  - *Phase Shift Masks*
  - *Off-Axis Illumination (OAI)*
  - *Optical Proximity Correction (OPC)*
  - *Computerized Resolution Enhancement*
  - *Immersion Lithography*
  - *Multiple Patterning*

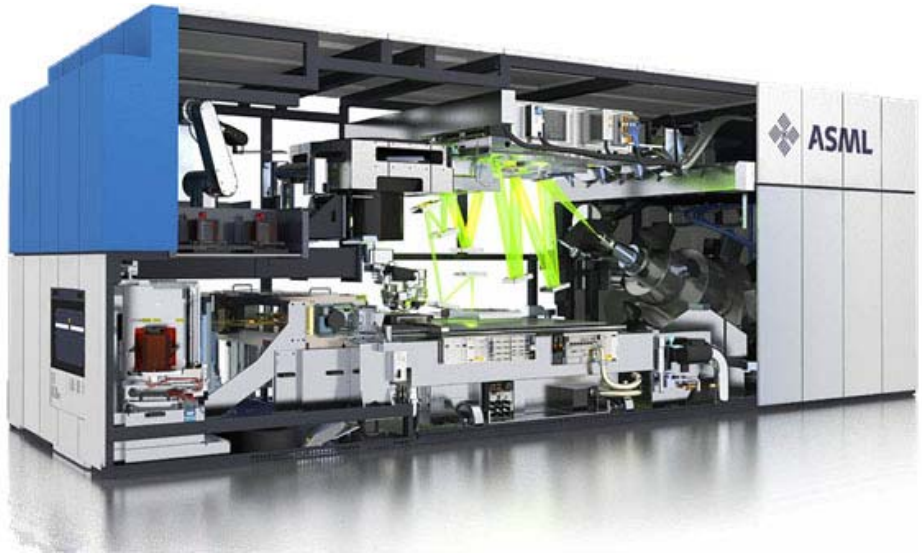
EUV Litografija

Extreme Ultra Violet



EUV Status	ASML/Zeiss	NIKON	Canon
Demonstration Tool	Installed 2006	Installed 2007	N/A
Pre-Production Tool	1st shipment 2010	N/A	N/A
Volume Production Tool	1st shipment 2012	?	N/A

EUV Status (2010) ?



"EUV – Forever Delayed?"

"ASML: EUV Chip Manufacturing Will Slip to 2015."

"Optical lithography will live forever…"

"No exponential is forever… but we can delay 'forever'" – Gordon E. Moore

Reference

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